In the Claims

Claims 1-75 cancelled.

76. (Amended) ~~A method for making a semiconductor device comprising a semiconductor substrate having a lowered effective electrical resistivity, the method comprising: in a first surface, forming a plurality of source regions of dopants of one polarity, said source regions all electrically connected together; in the substrate below the source regions forming a drain layer of dopants of the same polarity as the source regions; between the source regions and the drain layer, forming well regions of dopants of opposite polarity to define channels between the source regions and the drain layer; forming gate regions over the channels and between the source regions and the drain layer, said gate regions electrically connected together; forming a pattern of recesses extending from the second surface of the substrate into interior portions of the semiconductor substrate, said recesses located at chosen positions and having chosen shapes and chosen depths in the substrate; and forming resistivity-lowering bodies in the recesses, the resistivity-lowering bodies comprising a material having an electrical resistivity lower than an electrical resistivity of the semiconductor substrate.~~

A method for making a semiconductor device comprising a semiconductor substrate having a first surface and second, opposite and planar surface and a lowered effective electrical resistivity, the method comprising:

in the first surface, forming an one or more device active regions above the drain layer, said device active regions comprising one or well of dopants of a second and opposite polarity and in said wells one or more source regions of dopants of the first polarity, the source regions laterally spaced from each other;

forming gate regions over portions of the well regions between the source regions and the drain layer;

in the second, planar surface forming a highly doped drain region; and

in the second, planar surface of the substrate after forming the highly doped drain region, forming one or more resistivity-lowering bodies extending from the second, planar surface of the substrate into interior portions of the semiconductor substrate, the resistivity-lowering bodies comprising a material different than the

semiconductor substrate and having an electrical resistivity lower than an electrical resistivity of the semiconductor substrate.

77. (Amended) A method according to Claim 7752 wherein the step of forming the pattern of recesses comprises sawing or etching a recess into the surface of the substrate.

78. (Amended.) A method according to Claim 7752 wherein the step of forming the pattern of recesses comprises laser etching to form cylindrical recesses.

79. (Original) A method according to Claim 76 wherein the step of forming the pattern of recesses comprises forming a repeated pattern.

80. (Original) A method according to Claim 79 wherein the repeated pattern is a trapezoidal pattern.

81. (Original) A method according to Claim 76 wherein the recesses comprises a grid of intersecting trenches.

82.(Amended) A method according to Claim 76 further comprising forming an electrical contact layer on the second surface of the semiconductor substrate being electrically connected to one or more of the resistivity-lowering bodies ~~the at least one resistivity lowering body~~.

83. (Amended) A method according to Claim 76 wherein forming the resistivity-lowering bodies ~~at least one resistivity lowering body~~ comprises filling an associated recess.

84. (Previously presented) A method according to Claim 76 further comprising forming a barrier layer lining in at least one recess.

85. (Previously presented) A method according to Claim 76 wherein forming the resistivity-lowering body comprises forming said body using an electrical conductor having an electrical resistivity less than about $10^{-4}\Omega$-cm.

86. (Original) A method according to Claim 76 wherein forming the recesses and
associated resistivity-lowering body comprises forming the recesses and the associated resistivity lowering bodies to define a proportion of the semiconductor substrate area adjacent the at least one device active region no less than about 0.4 percent.

87.(amended) A method according to Claim 76 wherein forming the recesses and associated resistivity-lowering body comprises forming the recesses and the associated resistivity lowering bodies to extend into the semiconductor substrate a distance greater than about 25 percent of a thickness of the semiconductor substrate.

88. (Original) A method according to Claim 76 wherein forming the at least one recess and associated resistivity-lowering body comprises forming an array of recesses and associated resistivity-lowering bodies.

89. (Amended) A method according to Claim 88 wherein forming the array of recesses and associated resistivity-lowering bodies comprises forming the recesses ~~are arranged~~ in a grid pattern.

90. (Original) A method according to Claim 89 wherein forming the grid pattern comprises cutting trenches in the second surface of the semiconductor substrate.

91. (Original) A method according to Claim 76 wherein forming the at least one device active region comprises forming at least one device active region for a metal-oxide semiconductor field effect transistor (MOSFET).

92. (Original) A method according to Claim 76 wherein forming the at least one device active region comprises forming at least one device active region for an insulated gate bipolar transistor (IGBT).

93. (Original) A method according to Claim 76 wherein forming the at least one device active region comprises forming at least one active region of a microprocessor.

Claims 94-104 are cancelled.